Fortgeschrittenen Praktikum

Experiment-24

MOSFET

(**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor)

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1. Introduction

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are one of the fundamental elements in the semiconductor microelectronics industry. They provide the practical route towards digital switching applications at high frequencies and extremely dense integration in microelectronics. In this experiment, you will investigate the fundamental electronic properties of a MOSFET, firstly by studying the capacitance-voltage characteristics of a **M**etal **O**xide **S**emiconductor (**MOS**) junction and finally, by investigating the properties of a MOSFET. The MOS junction consists of three active materials with strongly differing electrical conductivity (a semiconductor, an insulator and a metal). Close to the semiconductor-insulator surface one can precisely tune the conductivity by applying a potential difference between the semiconductor and the metal. This so called “field effect” is used to switch electrical conduction through the MOSFET on and off.
Important properties of the bulk semiconductor (bandgap, doping, the influence of light etc.) and their influence through the applied electric field will be investigated. In particular, the so called “space charge” zone at the surface of the semiconductor will turn out to have a particularly strong influence on the properties of the device and we will study the physics behind its formation.

2 The MOS System

The MOS structure is essentially a capacitor that consists of three basis components: a semiconductor (here Silicon, bandgap ~1.12eV) onto which an insulator (here SiO_2, bandgap ~9eV) is grown by thermal oxidation before a metal film is deposited. (see. Fig 1). In this case, the semiconductor and the metal film form the two plates of the parallel plate capacitor, separated by the oxide dielectric.

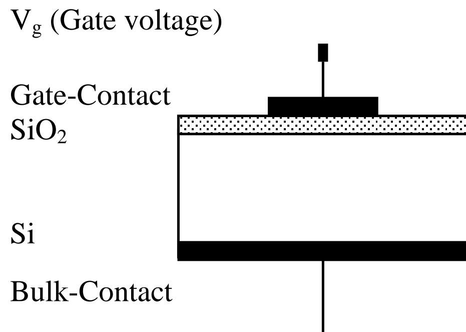
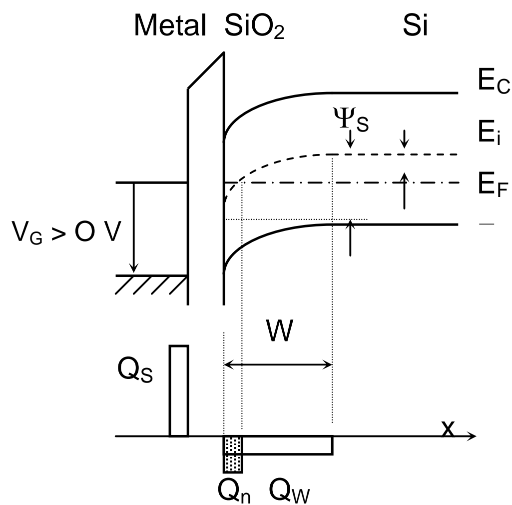


Fig 1 – Schematic physical structure of a MOS device.

By applying a potential V_G (the so-called gate voltage) between the semiconductor and the metal film, an electric field is created in this capacitor structure which extends through the insulator and into the semiconductor region. The magnitude of this field is proportional to the induced surface charge (Q_s) and is rapidly screened in the metal due to the high charge density but decreases more gradually in the semiconductor due to the lower free carrier density.

The schematic potential profile of a MOS structure is sketched if figure 2. The space charge layer at the interface is essentially determined by the charging and de-charging of defect centres in the vicinity of the interface as the applied voltage changes and the modification of the density of mobile charges. Since the magnitude of the externally applied electric field ($\sim 10^4$ V/cm → 10^6 V/cm) remains much smaller in comparison with the typical inter-atomic field ($\sim 10^8$V/cm), the applied field leaves the bandstructure of Silicon unaffected. In this case, the potential profile induced by application of the gate voltage acts in addition to the bandstructure and gives rise to a band bending Ψ_s in the space charge layer.



Q_S	Induced surface charge
Q_n	Inversion layer charge
Q_W	Space charge
W	Width of the space charge layer
Ψ_S	Surface band bending
Ψ_B	Separation between the Fermi level of the doped semiconductor compared with intrinsic material.

Fig 2 – Band profile and charge carrier distribution in the MOS structure.

The potential distribution can then be determined by solving the Poisson equation subject to the following overall boundary conditions:

(i) The electric field must vanish far into the interior of the semiconductor

(ii) The electric field at the surface is proportional to the total induced surface charge density. This also depends on the size of the energy gap, i.e. the separation between the conduction (E_c) and valence band (E_v) edges. The exact mathematical treatment is not complicated but rather lengthy. Interested students can find it the extract from the book *Physics of Semiconductors*, by Sze (handout 1)

Three distinct regimes of operation can be defined. The following discussion applies to the situation when the semiconductor is p-doped (The situation for n-doped material would be analogous, with the polarity of the voltage inverted)

Accumulation: In this case the gate voltage is negatively biased with respect to the semiconductor ($V_g<0$). The resulting negative charge in the metal has an influence on the majority carrier holes in the p-Silicon, attracting them towards the Si-SiO_2 interface. As a consequence, the bands in the semiconductor become bent toward higher energy due to the *accumulation* of holes close to the Si-SiO2 interface.

Depletion: In this case the gate electrode is weakly positively biased ($V_g>0$) such that the majority holes in the semiconductor are repelled from the Si-SiO_2 interface into the body of the semiconductor. This gives rise to a *negative* region of fixed space charge due to the ionized acceptors in the vicinity of the junction that tend to screen the electric field. The bands in the semiconductor are then bent to lower energy. The region of the semiconductor immediately adjacent to the SiO_2 becomes *depleted* of mobile charge carriers resulting in the formation of a semi insulating layer.

Inversion: In this case the gate is strongly positively biased ($V_g>>0$) such that the bands bend still further to lower energy when compared with the "depletion" situation discussed above. At the point when the midpoint of the bandgap (E_i) intersects with the Fermi level in the Silicon, more free electrons exist in the interface region than holes, a situation called *weak inversion*. As the conduction band edge approaches the Fermi level further, the density of free electrons at the surface grows exponentially until, at a threshold voltage V_T, it becomes huge since the conduction band minimum shifts below the Fermi level. For $V_g>V_T$ the electron density becomes very large at the interface and the system is said to be *strongly inverted*. The inversion layer consists of a very thin (few nm thick), two dimensional layer of electrons that is free to move in the two spatial directions parallel to the Si-SiO_2 interface. In the direction perpendicular to the interface these electrons are electrically isolated from the bulk p-doped material by the insulating depleted region. The system under strong inversion resembles a p-n junction.

For an ideal MOS-structure the bands should not be bent at $V_g=0$. However, due to the charging of defects in the semiconductor and surface states there is generally some band bending at $V_g=0$. One can restore the flat-band condition via a specially chosen gate bias $V_g=V_{FB}$ known as the flat band voltage. From the magnitude and sign of V_{FB} one can estimate the number of surface states and the polarity of trapped charge.

In this experiment we will investigate the space charge zone in the semiconductor using capacitance and conductivity measurements.

Part 1 - Capacitance Measurements of MOS diode

By solving Poisson's equation one can establish a relationship between the induced surface charge (Q_s) and the band bending profile at the surface in the space charge region (Ψ_s). The voltage profile across the Silicon dioxide insulator can then be determined from the relationship between Q_s and V_g.

Experimentally the development of the surface charge accumulation region can be probed by measuring the *differential capacitance* of the junction ($C_{tot}=dQ_s/dV_g$) as a function of V_g. In effect, this means that one modifies V_g by a small amount and measures the resulting modification of Q_s. We can easily think about the MOS system as a parallel plate capacitor (C / area = $\varepsilon_0\varepsilon_r/d$), in which the capacitance is a direct measure of the separation between the plates (d). In our case, the MOS system is analogous to two capacitors in series, one due to the oxide separating the semiconductor from the metal (C_{ox}) and the second due to the space charge region (C_{sc}). In this case, $1/C_{tot}=1/C_{ox}+1/C_{sc}=(t_{ox}/\varepsilon_0\varepsilon_r)+(w(V_g)/\varepsilon_0\varepsilon_r)$. Since t_{ox} is independent of the applied voltage but w depends strongly on V_g any variation of C_{tot} with V_g is due to the modification of the space charge region.

In the experiment, the differential capacitance will be measured by adding to a small AC modulation voltage $V_{AC}=V_0 \sin(\omega t)$ to the DC gate potential (V_g) and using the circuit show below in figure 3. This circuit consists of a known *reference* capacitor (C_M) in series with the *unknown* sample capacitance (C_{tot}). The mixed AC and DC potential is applied across the two capacitors in series and the AC voltage across the reference capacitor (V_M) is then selectively amplified with amplitude and phase sensitivity using a device known as a *lock-in amplifier*. In this way, the purely capacitive component of the voltage (with the correct phase relative to the modulation voltage) can be measured, from which we can determine C_{tot}.

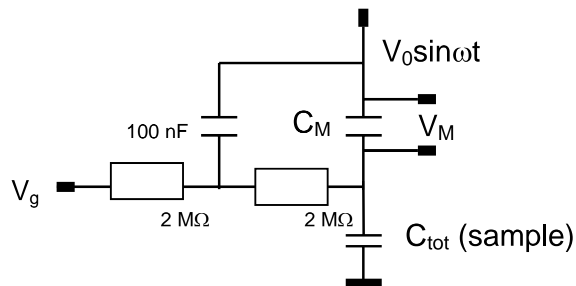


Fig.3: Circuit for the measurement of the sample differential capacitance

1) Stray capacitance and calibration of circuit.

First we need to gain familiarity with the equipment and apply the mixed AC and DC voltage to the sample. To do this set the modulation voltage on the oscillator to 200mV (peak-peak) at a frequency of 640Hz. You can check this with the oscilloscope supplied. We then have to estimate the stray capacitance of the voltage source, wires and circuit and "calibrate" the measurement circuit by replacing the sample capacitance with a series of known capacitors and making a calibration curve (use the standard capacitor box supplied). The correct way to connect the system is depicted of figure 4 below.

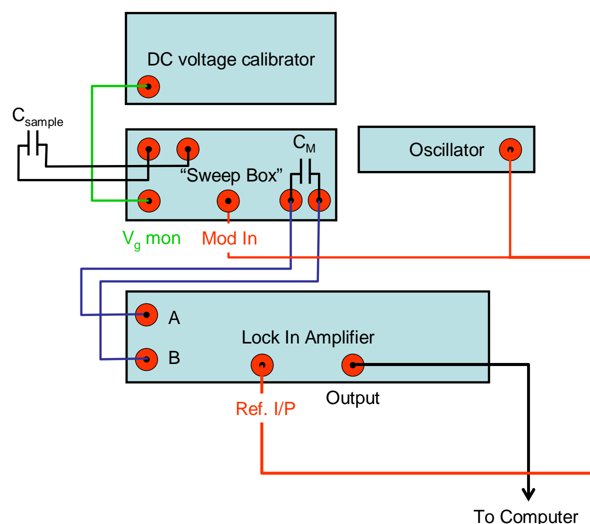


Figure 4 – schematic of circuit set up for differential capacitance measurement

To set the detection phase of the lock in amplifier, first replace the sample with a reference capacitance of 1nF. The voltage across this capacitor should then be measured using the lock in amplifier, having first set the phase very precisely to 90° (This can be done most easily by adjusting the phase control until there is zero output on the lock in and then turning the switch to adjust the phase by exactly 90° – increase the sensitivity to make sure the signal is zero!!) After obtaining zero output, shift the phase by 90° and disconnect the 1nF capacitor. The signal that you still measure on the lock in is due to the stray capacitance of the voltage source, circuit and wires and should be subtracted from all the measurement values you use later on. After this you should calibrate the output of the circuit using the capacitor switch box provided.

2) Connect the MOS sample. The gate voltage can be controlled using the DC voltage source provided. Start by stepping the voltage by hand between -8V and +8V. What happens? Decide on an interesting range of V_g and record a $V_M – V_g$ curve with the computer. You can then convert this to a C_{tot}-V_g curve using the calibration and stray capacitance measurement you obtained earlier by plotting the data using Microcal Origin. Make sure you set the delay time between measurements to be *longer* than the time constant setting of the lock in amplifier to prevent aliasing.

3) Record curves for different frequencies of ω=64, 640 and 6400Hz with and without illumination with the red LED provided. The LED can be switched on using the current source provided. For *each* frequency you will have to measure the stray capacitance and calibrate the measurement circuit.

Analysis

- Calculate the impedance of the measurement circuit (capacitive voltage divider). What relationship has to exist between ω and C_M such that the measured voltage is a direct measurement for C_{sample}?

- Determine the doping type of the sample (n or p?)

- Calculate the oxide thickness.
- Calculate the defect canter concentration from the ratio C_{min}/C_{ox} at 640Hz – see extra literature.
- Explain the observed frequency dependence.
- Explain the influence of above bandgap optical illumination.
- Determine the threshold voltage V_T and V_{FB}.
- Determine the ion concentration in the oxide.

Part 2 – Conductivity of the MOSFET.

Figure 5 below shows schematically the structure of an n-channel MOSFET (p-doped bulk Silicon) which is a three terminal device.

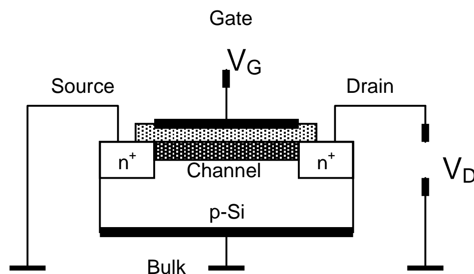


Fig 5 – Schematic of an n-channel MOSFET

The MOSFET consists of two strongly n^+ doped contact regions called the **source** and **drain** contacts. By applying a potential difference V_D (*drain voltage*) between the source and drain, we can measure the source-drain current (I_{SD}) that flows through the inversion layer close to the Si-SiO_2 interface. The source drain conductivity is strongly dependent on the applied gate potential, allowing the MOSFET to function as a switching device as follows:

- If the gate voltage (V_G) is tuned above threshold ($V_G>V_T$), an inversion layer is created below the gate electrode (as for the MOS system discussed above) and the measured source-drain resistance (R) should be low.

- If $V_G<V_T$, then the inversion layer vanishes and the source-drain resistance (R) increases dramatically due to "back to back" p-n diodes that form at the interface between the n^+ contact regions and the p-doped bulk semiconductor.

The dependence of I_{SD} on the gate voltage at a fixed source-drain voltage is known as the transistors *input characteristics* and one can determine the threshold voltage (V_T) from it.

The specific channel resistance R can be determined from:

$$R = \frac{W}{L} \cdot \frac{V_D}{I_{SD}} = \frac{1}{\sigma_s}$$

Where L and W are the length and width of the gate electrode respectively and σ_s is called the **specific channel conductivity**. In general, these parameters are related to the density of electrons (n) and holes (p) and their respective *mobilities* (μ_n and μ_p) by,

$$\sigma_s = e(n\mu_n + p\mu_p)$$

The two carrier mobilities in semiconductors are generally defined as the constant of proportionality between the drift velocity (v_d) and the strength of the electric field in the channel (E), i.e. $\mu = \frac{v_d}{E}$. In an n-channel MOSFET, n>>p and the channel conductivity can be written as $\sigma_s = en_s\mu_{eff}$ where n_s is the areal density of free electrons in the inversion layer of the channel and μ_{eff} is their "effective mobility". The effective mobility may differ from the bulk mobility since it depends strongly on the local free carrier density in the channel. If we know the relationship between the

carrier density (n_s) and the gate potential, we can re-arrange the preceding equations to obtain the following expression for μ_{eff}

$$\mu_{eff} = \frac{R}{en_s} = \frac{\frac{L}{W}.\frac{I_{SD}}{V_d}}{\frac{eQ_s}{LW}} = \frac{\frac{L}{W}.\frac{I_{SD}}{V_d}}{\frac{C_{ox}}{LW}\left(V_g - V_T)\right)} \quad \text{since } Q_s=C_{ox}(V_g-V_T)$$

This means that a measurement of the channel resistance, combined with knowledge of the dependence of n_s on V_g provides access to the density dependence of μ_{eff}. A related quantity, known as the field effect mobility (μ_{FE}) is defined via

$$\mu_{FE} = \frac{d\sigma_s}{dQ_s} = \frac{1}{e}.\frac{d\sigma_s}{dn_s}$$

By inserting the equation for σ_s in the above definition of the field effect mobility we can obtain the following relationship between μ_{FE} and μ_{eff}.

$$\mu_{FE} = \mu_{eff} + n_s.\frac{d\mu_{eff}}{dn_s}$$

It is clear that both mobilities are identical when μ_{eff} becomes independent of n_s, i.e. when $d\mu_{eff}/dn_s=0$.

Experimentally one can measure the field effect mobility in the following manner: a small AC modulation voltage is added to the DC gate potential to produce a time dependent modification of the surface charge dQ_s. The resulting modification $d\sigma_s$ of the conductivity can then be detected via the modulation of the source-drain current.
From the mobility one can obtain the so-called *momentum relaxation time* τ which is the average time between scattering events for charge carriers in the channel. The mobility is related to the momentum relaxation time by

$$\mu = \frac{e\tau}{m^*}$$

Where m^* is the so-called "effective mass" of an electron in Silicon $m^* \sim 0.2m_o$, where m_o is the free electron mass ($m_0=9.1.10^{-31}$ kg)

4) Measurement of the effective mobility

The effective mobility can be determined by measuring I_{SD} as a function of V_g. To do this, set $V_D=100mV$ and vary V_g in the range $-2V<V_g<+10V$. Make two series of measurements at 300K and liquid nitrogen temperature (77K)

5) Measurement of the field effect mobility

The field effect mobility can be measured by adding to the gate voltage a modulation voltage of 100mV at ω=64Hz. The frequency component of the voltage drop across a standard resistor R_s should then be measured using a lock in amplifier as depicted schematically in figure 6 below.

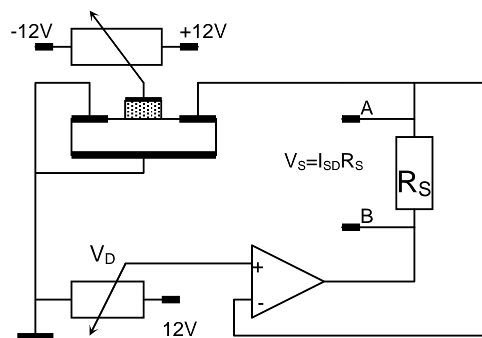


Figure 6 – Circuit for the measurement of I_{SD}.

As discussed above, the modification of I_{SD} as a function of V_d is directly proportional to the field effect mobility. Again, the measurements should be performed with a modulation voltage of $V_D=100mV$, V_g should be varied in the range $-2V<V_g<+10V$ and two sets of measurements should be recorded at 300K and 77K.

Analysis

- What is the relationship between V_G and n_s for $V_G>V_T$?

- You measured V_T at 77K and 300K – what causes the difference between the measured values?

- Using the ratio I_{SD}/V_D, determine μ_{eff} for a few values of n_s at 77K and 300K. Plot the dependence of μ_{eff} on n_s – can you explain your observations?

- Compare μ_{FE} as a function of n_s with the μ_{eff} (n_s) dependence plotted in the previous section (you may have to scale the data to plot them on the same curve)

- Determine the scattering time for maximum μ_{eff} at 300K and 77K.

Part 3 – The pinch off effect in the MOSFET

Until now we have only considered the situation when V_d is small in comparison with V_G. Now it is interesting to investigate the situation when V_G~V_d. For this purpose, we will study the dependence of the source drain current on the drain voltage at a *constant* gate potential – the so called **output characteristics** of the MOSFET. Providing that V_d remains smaller than V_g, I_{sd} varies linearly with V_d. However, as V_d becomes comparable to V_g, I_{sd} begins to saturate and, eventually, becomes independent of V_d. This behaviour and its origins - the so-called **pinch off effect** - are sketched on figure 7 below.

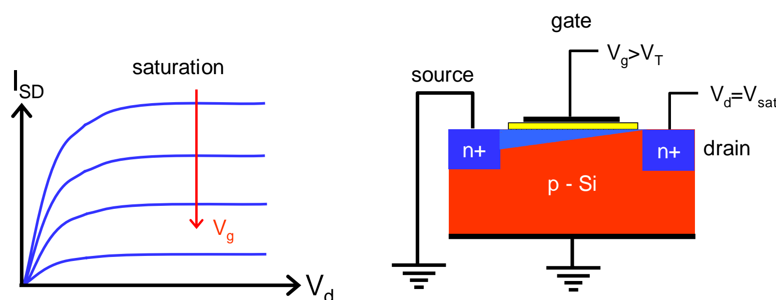


Figure 7 – The MOSFET output characteristics and the device at pinch off.

The pinch off arises from the following reason: the source and semiconductor bulk material are fixed at a common earth potential. If we now make the voltage applied to the gate and drain electrodes similar, then there must be zero electric field in between the gate and inversion layer at the drain electrode. In this case $n_s \to 0$ in the vicinity of

the drain contact at the so-called "pinch off" point. Carriers arriving at the pinch off point must then diffuse into the drain contact to complete the circuit. As V_d increases further, the pinch off point moves towards the source contact and the channel resistance increases such that I_{sd} remains constant.

6) Record a set of output characteristics as a function of gate potential.

Analysis

- Why does the source drain current not completely saturate for $V_d>V_{dsat}$?

- Quantitatively plot the dependence of V_{dsat} on V_g and explain your findings.

Safety instructions:

In case of emergencies, please contact the TUM fire department: 112

Emergency: 112 (fire department)

General instructions:

Please acquaint yourself with the safety facilities before working in the lab. Localize the closest fire extinguisher / the closest fire blanket. Where is the closest fire alarm? Where is the emergency exit? Where can you find instructions for accidents? Who do you have to contact?

Lab space has to be kept clean. Everyone keeps his own place tidy. Food and drinks are not permitted to be brought into the lab. When working with chemicals, contamination and toxication is possible.

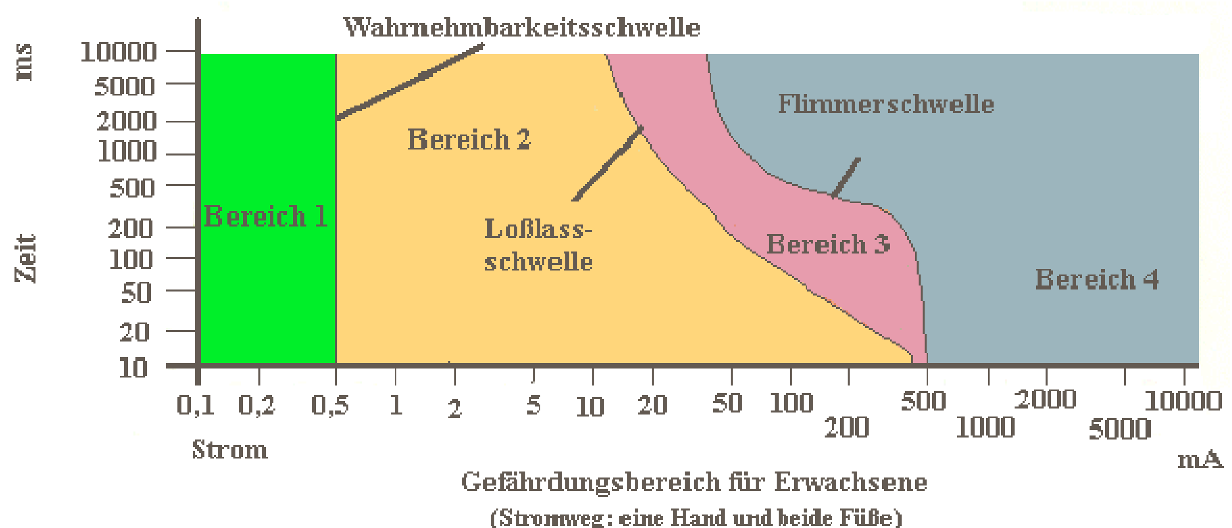
Fruit juices are very acidic and corrode electronics immediately. Please wash your hands before working with electronic equipment.

Individual operations must not lead to an increased safety risk for others (Cleaners, coworkers, visitors).

Electricity:

Current pulses:

E.g.: With a resistance of approx. 1kOhm (hand-feet), a voltage of 50V is sufficient to cause mortal danger (see diagram!).



Range 1: Alternating currents in this range will not be noticed by most people.

Range 2: A slight tingle can be noticed, but also painful spasms can occur. Bodily injuries are hardly possible.

Range 3: The current source cannot be released due to muscular spasms.

Range 4: Strong injuries and in many cases mortal effects, e.g. due to ventricular fibrillation.

Body resistance (minimal):
Hand - hand approx. 650 Ω
Hand - foot approx. 1300 Ω
Hand - feet approx. 975 Ω
Hands - feet approx. 650 Ω

The resistance of the skin is a few thousand Ohm, but at high voltages it can drop down to zero.

ESD (Electro Static Discharge):

Every person can easily be charged to a several 1000V simply by moving. Quite often, active electric elements can be destroyed with a few volts only. This can also happen, when a part of the body is in the proximity of the device without actually touching it. When working with sensitive measurement devices or with electric elements of all kinds, a ground strap has to be worn. This can prevent costly repairs.

Working with liquid Nitrogen:

- Contact with liquid Nitrogen can lead to cryogenic burns or freezes. Always be careful, that no liquid can enter the shoes.
- In rooms with insufficient ventilation, filling and decantation of liquid Nitrogen can lead to high concentrations of Nitrogen in the breathable air and displace the Oxygen. Possibility of acute suffocation!
- Enclosure of liquid Nitrogen into inappropriate containers without pressure compensation can lead to detonation of the container. Containers made of plastic will be subject to cold embrittlement. Endangerment due to shrapnels.
- Filling stations may only be installed in rooms with good ventilation. The faucets should be self-locking. Fill liquid Nitrogen only in well ventilated rooms.
- Always use safety goggles and gloves when filling or handling liquid Nitrogen.
- Use face protection when spraying is possible.
- Do not ride in the same elevator as the liquid Nitrogen container.